Low Voltage Current Conveyor based on OTA

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Abstract

In this work, a different connection of operational amplifier used to realize a second generation current conveyor CCII. The need of low voltage current conveyor guided to invent various circuits as design of low voltage current conveyor, this paper focused on some topologies from literature, and simulated by orcad 9.2 using CMOS 0.7Um.

This connection reveals that the circuits exhibits a good degree of accuracy in its current following capability as is expected of a current conveyor even at the unity gain frequency.

1. Introduction

To date a variety of designs used to construct CMOS CCIIs, This paper demonstrate a variety of CMOS operational amplifier can be converted into a Low voltage CCII. Our contribution is study the characteristics of an operational amplifier derived CCII-working in low voltage.

This paper demonstrated the conversion of an operational amplifier to a second-generation current conveyor. The conversion technique also reveals a simple way of developing a current conveyor. Moreover it suggests an elegant approach to making a current conveyor of good performance that will be pertinent for use in low voltage circuits which are compatible with today's diminishing power supply for VLSI circuits. the generality of the technique cannot be over-emphasized as the achievable bandwidth of the resulting device is that of the operational amplifier used in the design.[1,2].

Different topologies have been discussed and compared each other with respect to the current transfer ratio, voltage dynamic range, and the resistance at terminal X node.

2. Principle of operation

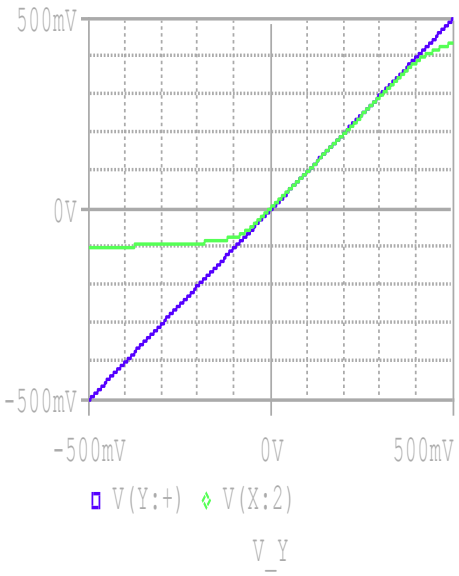
Operational amplifier is used to implement the unity gain buffer between the Y and X inputs. The X input current ix, is sensed by simply duplicating the buffer's output transistors, and extracting the X current from them as iz., the current iz should be a copy of the ix. Since no additional transistors need to be inserted between the

operational amplifier and the supply rails, the approach will not increase the minimum operating voltage over that of the operational amplifier core. In addition, the voltage follower is based on an operational amplifier and so will maintain all the benefits (and disadvantages) of such a circuit (a good voltage follower at the cost of lower bandwidth). [3-5].

3. Simulations of CCII Topologies

To verify the results of selection of designs of operational amplifiers from the literatures were used to make the buffer required in the transformation process to the CCII- .Simulations were carried out with Orcade 10.5 using 0.7 μm CMOS process model were all the operational amplifiers designed to work around 1V supply.

Let us see the following circuit Figure 1-a which is able to operate at only ±1V total supply voltage, the lower supply voltage has performed through the improvement of a different biasing circuit for X and Z output stages, the output stages in this circuit not dependent on supply voltage.



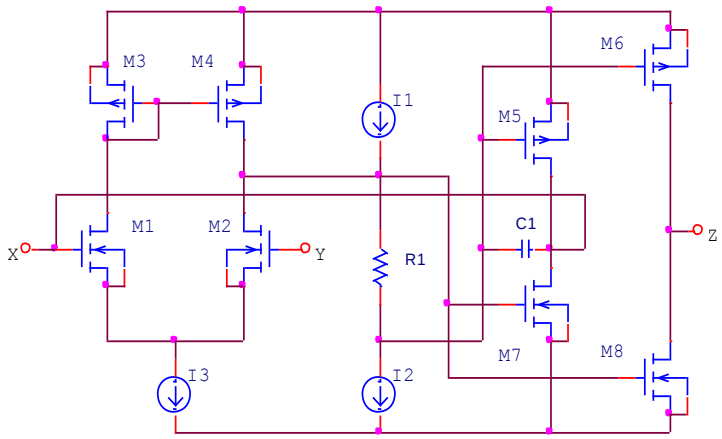
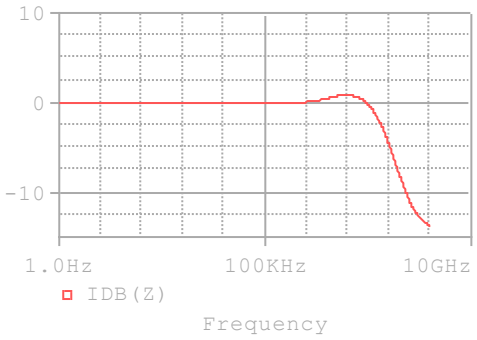


Figure 1 a) Class AB CCII with improved biasing.



b) Vy and Vx voltages.

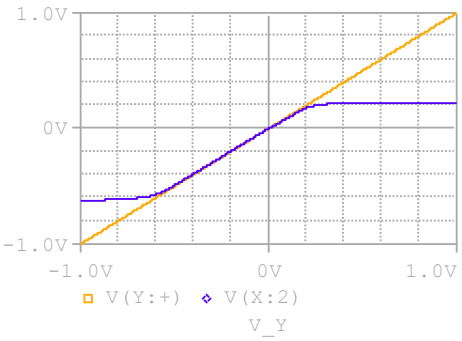
[1]

There is a limitation for dynamic range at negative voltages, because X node voltage level cannot foll ow Y node as shown in. since this CCII is based on a n-type differential pair, the dynamic range is more extended towards the positive voltages (-80mv to 350mv).

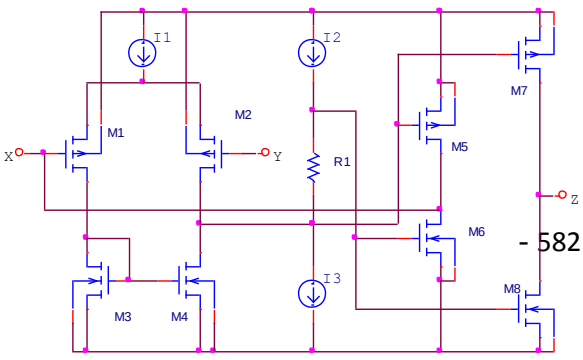
[2]

c) Current transfer ratio iz/ix in dB.

It's possible to find similar results considering the solution based on the complementary p-type differential pair The supply voltage used cannot have lower than one threshold voltage PMOS transistor which is about 0.8V in AMIS 0.7 um CMOS technology, the simulation proofed the dynamic range is more extended towards the negative voltages as depicted in figure 2- b,c



b) Voltage follower between X and Y nodes



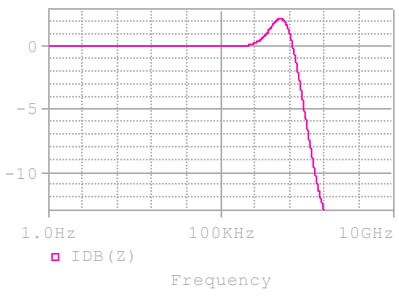
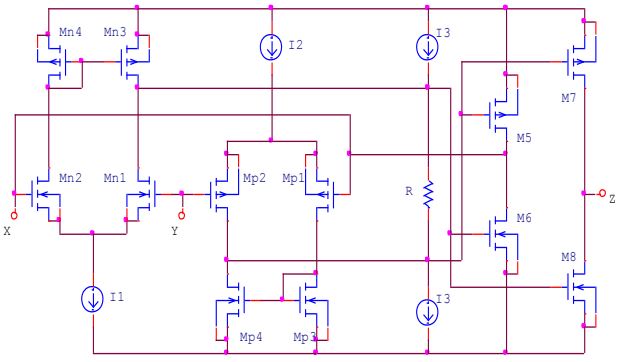


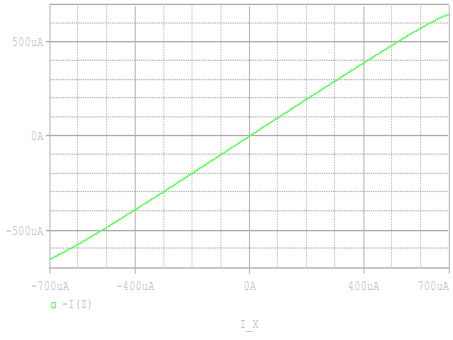
Figure a) Class AB CCII based on p-type differential pair.

c) Current transfer between x and z nodes.

The two last topologies can be merged together to design a rail to rail CCII, as seen in

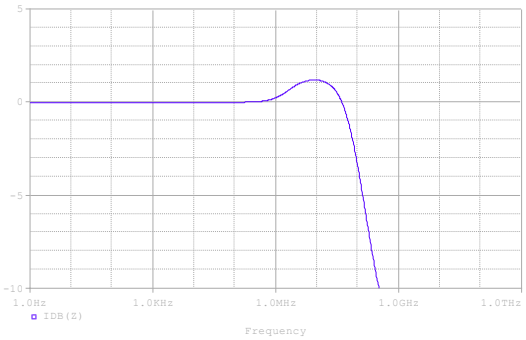
the basic concept is to use both differential pairs, the n-type based and p-type based, connecting the two single ended outputs to the gates of output stages.

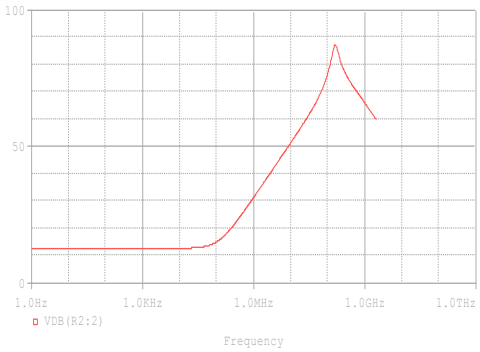




b) Vy and Vx voltages.

c) Current linearity in output node.





c) Current transfer ratio.

d) x node parasitic impedance

By placing the two complementary pairs in parallel, it has been possible to design a rail to rail OTA based CCII, which shows good performance at LV supplies. The voltage follower extended to both positive and negative directions (-600mV, 550mV) with 80MHz current transfer ratio, low input resistance 12Ω, and excellent current linearity between x and z nodes, simulation results shown in .

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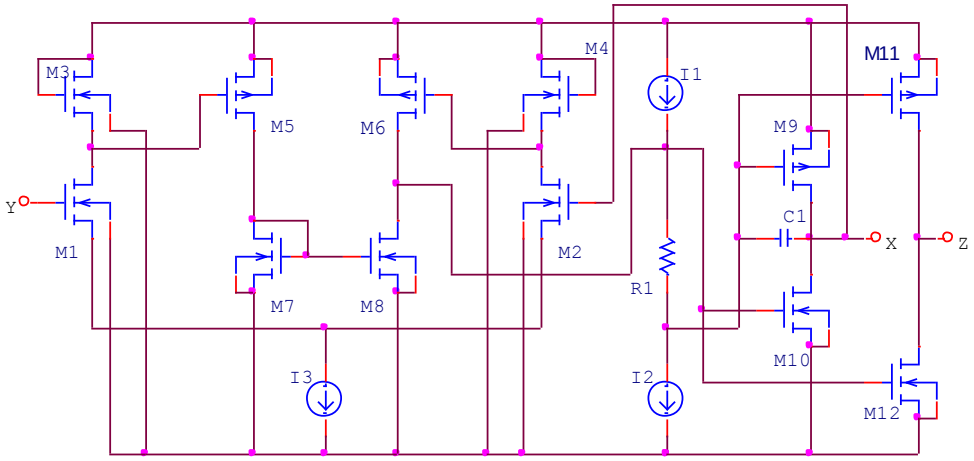


[3] Figure 4. LV OTA based CCII.

Another Second generation current conveyors are implemented starting from an OTA topology, using gained output stages (class AB inverter) and applying a proper feedback, as shown in the schematic in Figure which is able to operate at value ± 1V supply voltage level. For this CCII, Av and Ai parameters are given by the following expressions.

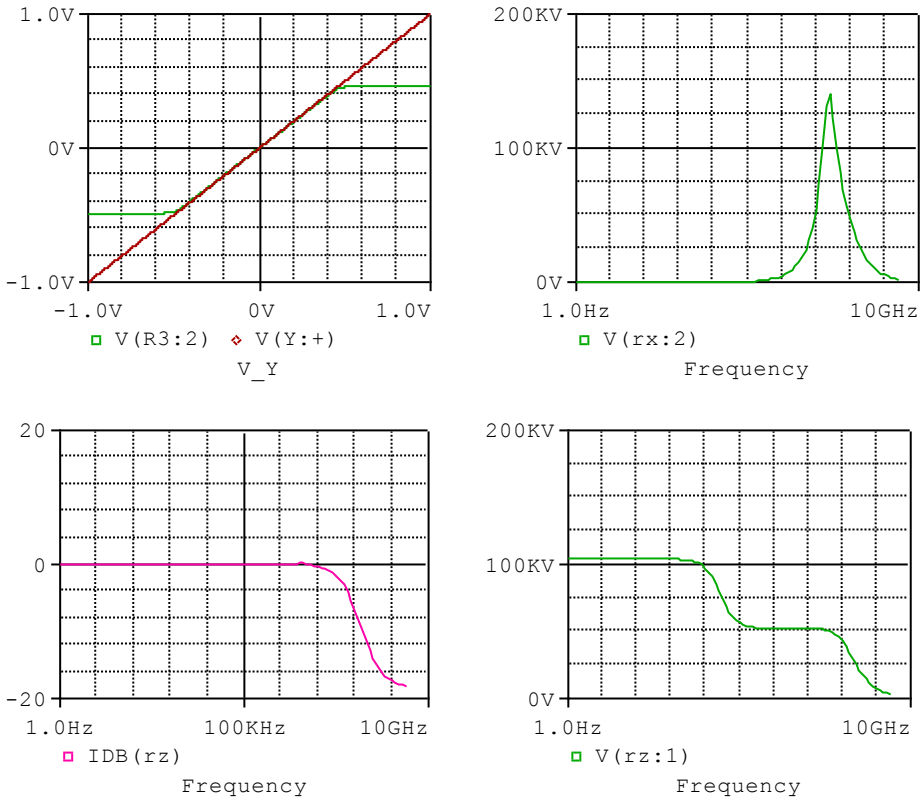
$$A_v = \frac{V_X}{V_Y} \cong \frac{g_{m1}}{g_{m2}} \cong 1 \quad 1.$$

$$A_i = \frac{I_Z}{I_X} \cong \frac{gm11 + gm12}{gm9 + gm10} \cong 1 \quad 2.$$

The parasitic impedance levels at X and Z nodes are

$$r_x \cong \frac{2}{g_{m2}(g_{m9} + g_{m10})} \quad 3.$$

$$r_z = \frac{r_{O11} r_{O12}}{r_{O11} + r_{O12}} \quad 4.$$



[4] Figure5 LV OTA based CCII simulations.

This circuit is solution for low voltage supply, it showing acceptable characteristic, dynamic range is -380V to 210V Figure. The parasitic resistance of input rx is very low as its demanded in CCII and from figure – rz acceptable that showing high value.

4. CONCLUSION:

CMOS Class AB configurations of CCIIs based on n-type and p-type differential pair have been presented, simulation shows that the dynamic region extended toward either positive value for n-type or negative for p-type, to achieve both of them LV rail to rail OTA based CCII designed and approved better dynamic range and linearity.

Another topolgy have been discussed and compared with respect to the voltage transfer gain, the resistance at terminal x, CMOS OTA configurations using AB inverter of CCIIs have been presented, compared with rail to rail based on class AB n,p-type circuits can achieve better performance in terms of accuracy and linearity, which are very important parameters for conveyors used as input stage in current-mode amplifiers. Improved performance is achieved by using gained output stages (class AB inverter) and applying a proper feedback in the voltage buffer.

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